

# **FPGA Resource Usage**

For WF C Series Modules

# **Abstract**

This application note describes how to check if your software design with a WF C series module will fit on a specific cRIO. It will also provide a benchmark list for WireFlow's C series modules and discuss some considerations that affects the FPGA usage.

# **Problem**

How can I verify that my FPGA design with a WireFlow C series module will fit on a certain cRIO?

## Solution

The FPGA usage of a specific software and hardware combination is affected by multiple factors such as:

- FPGA type and size
- Compilation options
- If the cRIO model has cDAQ support
- Version on compilation tools
- The random starting point for FPGA code placement

Hence it is impossible to derive an exact figure that defines the FPGA usage of a specific C series module.

For customers that are uncertain on whether their application will fit on a specific FPGA with a WireFlow C series module it is recommended to make a test-build. Note that no hardware is needed to make a test build.

To make a test-build with a WireFlow C series module, the module drivers must be installed. They are available free of charge as .vipm-packages on LabVIEW tools network and on <a href="http://www.wireflow.se/">http://www.wireflow.se/</a>

After driver installation, the module can be added just like any other C series module. To add a module or target without having access to the hardware, use the "New target or device" radio button as shown in figure 1. Compilation can then be performed as usual.

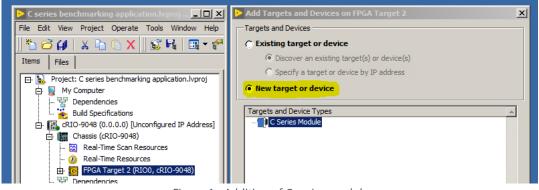


Figure 1 - Addition of C series module

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# Benchmark figures

All of WireFlow's C series modules are benchmarked before release to verify that 8 modules can be fitted in at least one of NI's cRIO chassis. A basic test application that allows read and write of all I/O-nodes for each module on the FPGA vi's front panel is used.

Experience has shown that the WF 3169 is the module that currently consumes the most FPGA resources in WireFlow's C series range. It can therefore be assumed that the WF 3144/3132/3154/3168 will fit in each chassis where the WF 3169 fits.

The following configurations have been tested by WireFlow with a basic I/O-application, sorted on FPGA type and size.

#### Artix-7 75T with cDAQ support (cRIO-9056)

8x WF 3169 modules (LabVIEW 2018 SP1)

#### Kintex-7 70T (cRIO-9035)

8x WF 3144/3132/3154/3168/3169 modules (LabVIEW2017 SP1)

#### Kintex-7 70T with cDAQ support (cRIO-9045)

8x WF 3144/3132/3154/3168 modules (LabVIEW 2017 SP1)

7x WF 3169 modules (LabVIEW 2017 SP1)

8x WF 3169 modules (LabVIEW 2018 SP1)

#### Kintex-7 160T with cDAQ support (cRIO-9048)

8x WF 3169 (LabVIEW 2017 SP1)

# Recommendations

Use the latest LabVIEW version/Xilinx compilation tools. For example, it's been noted that LabVIEW 2018/Vivado 2017.2 (64-bit) in some cases produce smaller FPGA code than LabVIEW 2017/Vivado 2015.4 (64-bit).

If choosing between two cRIO:s with the same FPGA, the models with cDAQ support can use up to 10% more FPGA resources if 8 slots are populated with modules. If not needed, it is therefore recommended to use a cRIO without cDAQ support.

### **External Links**

List of current cRIO-models and their FPGA configuration <a href="https://www.ni.com/crio">www.ni.com/crio</a>

List of FPGA types and configurations on cRIO-models (current and legacy) <a href="http://www.ni.com/product-documentation/54503/en/">http://www.ni.com/product-documentation/54503/en/</a>

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