Mixing WF and NI Modules in RIO chassis

Abstract

ScanEngine access is not directly accessible for Third-Party modules, but this Application note shows how to mix ScanEngine access for NI modules with more low level I/O access to a WireFlow C Series module.

WF 3144 NI Modules

Introduction

C Series modules in a RIO chassis can be accessed in either Scan Mode or FPGA mode, and many users find it very convenient to use the Scan Mode. This mode is however not available for all type of modules; Third-party modules, such as the WireFlow modules, are not directly accessible in the Scan Mode. Fortunately, it is possible to add third-party modules to the system and still access the NI modules in Scan Mode.

This application note will outline two different approaches to mix WireFlow modules with NI modules in a single C Series chassis:

- WireFlow modules accessed by using FPGA Read/Write method
- WireFlow modules accessed by User Defined Variables

In both cases all the remaining slots in the chassis will be available for ScanEngine access to NI modules, and it is even possible to switch to other NI modules without FPGA recompilation. The example code is available as a zip-file from wireflow.se/downloads (AB0057-057 AN4 Mixing WF and NI modules examples.zip)

The FPGA Read/Write approach allows WireFlow to distribute precompiled FPGA bitfiles to customers that doesn't have the LabVIEW FPGA toolkit. These customers can then use the WireFlow module using Read/Write methods and just point to the pre-compiled bit-file when the FPGA resource is opened. (see NI Support, Download a Bitfile to My Target Without LabVIEW FPGA)

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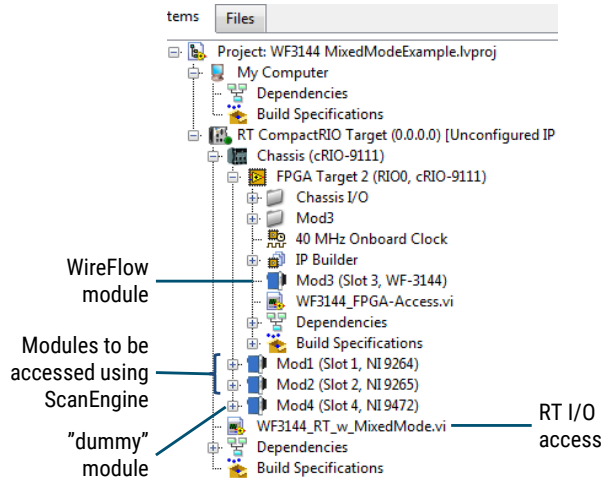
The User Defined Variables approach is very convenient since all I/O are accessed in the same way, and it is the preferred way to access third party modules when used in an EtherCAT slave chassis.

In the end it is up to the end-user of the module to determine which approach is best suited for the current application.

Accessing by Read/Write methods

In this example the ScanEngine access to the NI modules is mixed with access to the WF-3144 module by Read/Write methods.

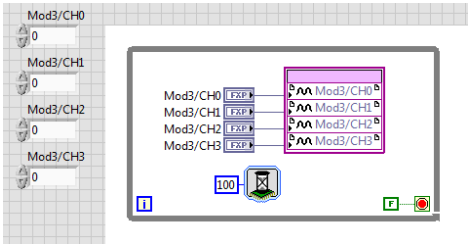
The trick is to add the WF modules under the FPGA target and add the modules for ScanEngine access directly under the chassis. Also add dummy modules (basically any NI module) to all empty slots, since this will force the FPGA compilation to add ScanEngine support even for empty slots.



Next thing is to create a very simple FPGA VI that accesses the WF modules and put access controls on the FP.

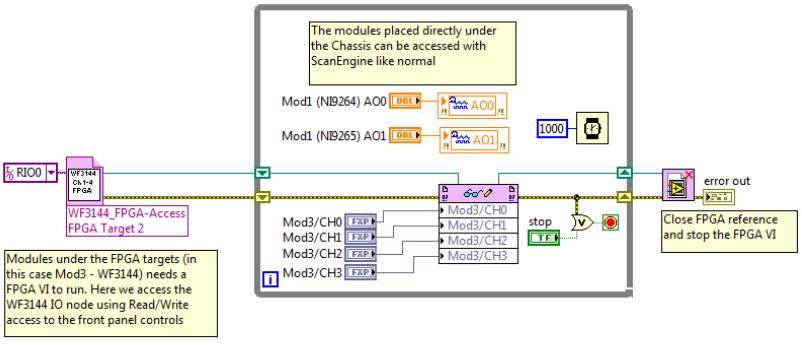
Once this FPGA VI has been compiled, all chassis I/O can be accessed within a single VI from the host. Here the WireFlow modules are accessed using the FPGA Interface methods:

- Open FPGA VI reference
- Read/Write control
- Close FPGA VI reference



The NI modules are accessed using ScanEngine, and the Read/Write node automatically shows the items that can be accessed for the WF modules (that are on the FPGA VI front panel).

Using this technique, an application can be created that use a mixture of ScanEngine access to NI native modules and FPGA Read/Write access to WireFlow modules.



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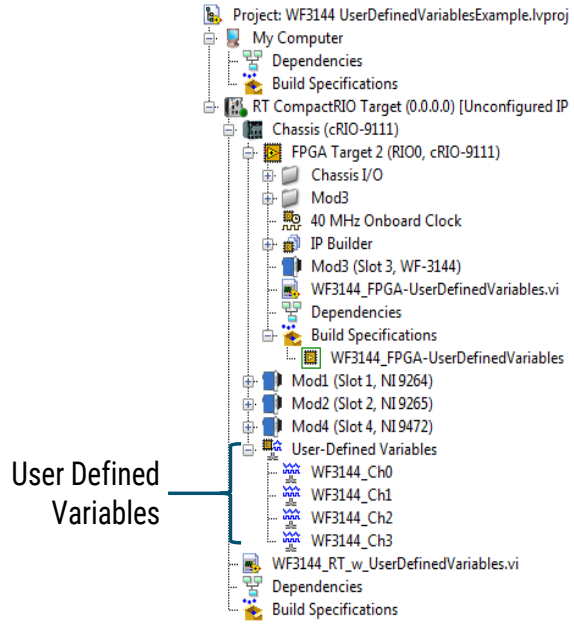
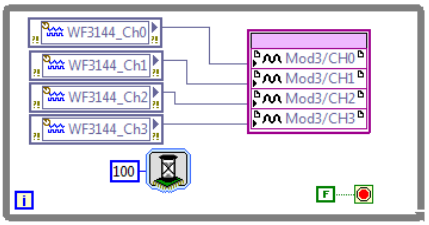
Access by “User Defined Variables”

If ScanEngine access to the WireFlow module is required, e.g. for access in an EtherCAT chassis, the previous project must be modified with User Defined variables

User Defined Variables are added by right-clicking the Chassis in the project. Each User Defined Variable has to be configured in terms of data type and direction, i.e. Host to FPGA or vice versa. Once all the variables have been added, they will show up in the project, and will be accessible in both RT and FPGA code, just like any ScanEngine variable.

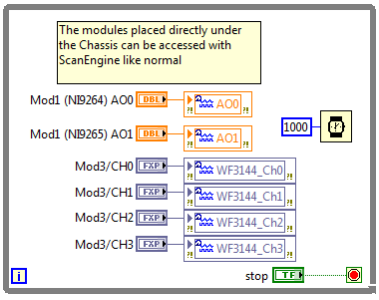


Make sure that the data type of the User Defined Variabel is correctly matching the data type of the I/O node on the FPGA, e.g. the WF 3144 is using a fixed-point data type with 26bits (20 integer bits).



The FPGA VI accesses the User Defined Variables like Scan Engine I/O, and connects them to the corresponding I/O nodes (see block diagram on the left). When using User Defined Variables it is not necessary to add front panel items to the FPGA VI, since all values are passed using the ScanEngine/User Defined Variables.

The only difference for the RT code compared to Read/Write node access is that the WireFlow module is accessed with the User Defied Variables, very much like the ScanEngine Variables



The ScanEngine background process is now used to pass all data between RT and FPGA.

User Defined Variables are also very useful when an EtherCAT slave chassis is used, because they allow convenient access to a third-party module as well as derived data (e.g. smart sensors).

Use this technique if the preferred access method is ScanEngine, or if the WireFlow module is to be accessed on an EtherCAT bus.

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